Claims

[c1] 1. A method of forming a solder bump connection at a metallic bonding pad surface of a semiconductor chip, said method comprising the steps of:

a) forming a patterned passivation layer upon said metal bonding pad surface, said patterned passivation layer including an opening at said metallic bonding pad surface to define a location for said solder bump connection;

b) forming a barrier material stack including top and bottom conductive material layers upon said patterned passivation layer, said barrier material stack conforming to a surface of said patterned passivation layer;

c) removing top conductive material layer portion of said stack adjacent said solder bump connection location so that a top conductive material layer portion at said solder bump connection location defines a surface that is substantially coplanar with a surface of remaining bottom conductive material layers adjacent said solder bump connection location;

d) forming a patterned resist material layer upon said substantially coplanar surface, said patterned resist material layer including an opening at said defined solder bump connection location;

e) forming a diffusion barrier layer upon said substantially coplanar surface defined by said patterned resist material layer opening;

f)providing solder material upon a surface of said diffusion barrier layer and between patterned walls defining said patterned resist material layer opening;

g) removing the patterned resist material layer and removing remaining bottom conductive material layer portions of said barrier material stack under said patterned resist layer; and,

h) reflowing the solder material to form said solder bump connection, wherein said bottom conductive material layer adjacent said solder bump connection exhibit decreased amount of undercut under said diffusion barrier layer to enable reduced pitch and increased mechanical stability of said solder bump connection.

[c2] 2. The method of forming a solder bump connection as claimed in Claim 1, wherein said step of removing a portion of said top conductive material layer includes implementing chemical mechanical polishing of said top conductive material layers to stop on said bottom conductive material layer of said barrier material stack adjacent said solder bump connection location.

[c3] 3. The method of forming a solder bump connection as claimed in Claim 1, wherein said step g) of removing remaining lower conductive material layer portions of said barrier material stack includes implementing a wet etch, wherein a total etch time for removing said remaining bottom conductive material layer portions is reduced due to prior removal of said top conductive material layer portions adjacent said solder bump connection location.

[c4] 4. The method of forming a solder bump connection as claimed in Claim 1, wherein said barrier material layer stack further includes an intermediate conductive material layer between said top and bottom conductive material layers, said step c) of removing upper conductive material layer portions further includes the step of implementing a CMP of said top conductive material layer adjacent said solder connection location until said intermediate conductive material layer of said barrier material stack becomes substantially coplanar with said top conductive material layer solder at said solder connection location.

[c5] 5. The method of forming a solder bump connection as claimed in Claim 1, wherein said step f) of providing solder material includes implementing an electroplating technique for depositing said solder material.

[c6] 6. The method of forming a solder bump connection as claimed in Claim 1, wherein said step a) of forming a patterned passivation layer upon said metallic bonding pad surface includes providing a single via opening at said metallic bonding pad surface.

[c7] 7. The method of forming a solder bump connection as claimed in Claim 1, wherein said step a) of forming a patterned passivation layer upon said metal bonding pad surface includes providing multiple via openings at said metal bonding pad surface.

[c8] 8. The method of forming a solder bump connection as claimed in Claim 6, wherein said step a) of forming a patterned passivation layer further includes the step of forming a via bar opening adjacent said single via opening at said metallic bonding pad surface, said low resistance seed layer facilitating electroplating.

[c9] 9. A solder bump connection at a surface of a metallic bonding pad of a semiconductor chip comprising:

a patterned passivation layer formed upon said metal bonding pad surface, said patterned passivation layer including an opening at said metal bonding pad surface defining a location for said solder bump connection;

a barrier material stack formed above said patterned passivation layer and including top and bottom conductive material layers, portions of said top conductive material layer portion adjacent said solder bump connection being removed such that a top conductive material layer at

said solder bump connection location includes a surface that is substantially coplanar with a surface of remaining bottom conductive material layer portions adjacent said solder bump connection location;
a diffusion barrier layer formed upon said substantially coplanar surface at said solder bump connection location; and,
a solder bump formed upon a surface of said diffusion barrier layer,
wherein portions of said bottom conductive material layer adjacent said solder bump connection exhibit decreased amount of undercut under said diffusion barrier layer to enable reduced pitch and increased mechanical stability of said solder bump connection.

[c10] 10. The solder bump connection as claimed in Claim 9, wherein said patterned passivation layer comprises one or more passivation material layers.

[c11] 11. The solder bump connection as claimed in Claim 9, wherein said metallic bonding pad comprises material including one of Cu or Al.

[c12] 12. The solder bump connection as claimed in Claim 9, wherein said metal bonding pad is formed in a low-k interconnect dielectric material layer.

[c13] 13. The solder bump connection as claimed in Claim 9, wherein said top conductive material layer includes Cu and a lower barrier material layer comprises material including Ti-W.

[c14] 14. The solder bump connection as claimed in Claim 9, wherein said barrier material layer stack further includes an intermediate conductive material layer between said top and bottom conductive material layers, said top conductive material layer being substantially coplanar with said intermediate conductive material layer adjacent said solder connection

location.

[c15] 15. The solder bump connection as claimed in Claim 14, wherein said intermediate conductive material layer comprises CrCu.

[c16] 16. The solder bump connection as claimed in Claim 9, wherein said formed patterned passivation layer includes a single via opening at said metallic bonding pad surface.

[c17] 17. The solder bump connection as claimed in Claim 9, wherein said formed patterned passivation layer includes multiple via openings at said metal bonding pad surface.

[c18] 18. The solder bump connection as claimed in Claim 16, wherein said formed patterned passivation layer further includes a via bar opening adjacent said single via opening at said metal bonding pad surface.

[c19] 19. A method of forming a solder bump connection at a metallic bonding pad surface of a semiconductor chip, said method comprising the steps of:

a) forming a patterned passivation layer upon said metal bonding pad surface, said patterned passivation layer including two or more via openings at said metallic bonding pad surface to define a location for said solder bump connection;

b) forming a barrier material stack including top and bottom conductive material layers upon said patterned passivation layer, said barrier material stack conforming to a surface of said patterned passivation layer;

c) removing top conductive material layer portions of said barrier material stack between each of said two or more via openings and adjacent said solder bump connection location so that a remaining top conductive material layer portions at said via openings of said solder bump

connection location includes a surface that is substantially coplanar with a surface of said remaining bottom conductive material layer adjacent said solder bump connection location;

d) forming a patterned resist material layer upon said substantially coplanar surface, said patterned resist material layer including an opening at said defined solder bump connection location;

e) forming a diffusion barrier layer upon said substantially coplanar surface defined by said patterned resist material layer opening;

f) providing solder material upon a surface of said diffusion barrier layer and between patterned walls defining said patterned resist material layer opening;

g) removing the patterned resist material layer and removing remaining bottom conductive material layer portions of said barrier material stack under said patterned resist layer; and,

h) reflowing the solder material to form said solder bump connection, wherein portions of said bottom conductive material layer adjacent said solder bump connection exhibit decreased amount of undercut under said diffusion barrier layer to enable reduced pitch and increased mechanical stability of said solder bump connection.

[c20] 20. A method of forming a solder bump connection at a metallic bonding pad surface of a semiconductor chip, said method comprising the steps of:

a) forming a patterned passivation layer upon said metal bonding pad surface, said patterned passivation layer including a first via opening at said metallic bonding pad surface to define a location for said solder bump connection, and a second via opening adjacent said solder bump connection location to define a dummy via location;

b) forming a barrier material stack including top and bottom conductive material layers upon said patterned passivation layer, said barrier material stack conforming to a surface of said patterned passivation layer;
c) removing top conductive material layer portions of said barrier material stack adjacent said solder bump connection location and said dummy via location so that a remaining top conductive material layer portion at said solder bump connection location and at said dummy via location defines a surface that is substantially coplanar with a surface of a remaining bottom conductive material layer adjacent said solder bump connection and dummy via locations;
d) forming a patterned resist material layer upon said substantially coplanar surface, said patterned resist material layer including an opening at said defined solder bump connection location;
e) forming a diffusion barrier layer upon said substantially coplanar surface defined by said patterned resist material layer opening;
f) providing solder material upon a surface of said diffusion barrier layer and between patterned walls defining said patterned resist material layer opening;
g) removing the patterned resist material layer and removing remaining bottom conductive material layer portions of said barrier material stack under said patterned resist layer; and,
h) reflowing the solder material to form said solder bump connection, wherein portions of said bottom conductive material layer adjacent said solder bump connection exhibit decreased amount of undercut under said diffusion barrier layer to enable reduced pitch and increased mechanical stability of said solder bump connection.

[c21] 21. The method of forming a solder bump connection as claimed in Claim

20, wherein said step f) of providing solder material includes implementing an electroplating technique for depositing said solder material, said remaining upper conductive material layer portion at said dummy via location enabling a plating of solder with increased uniformity.